ABSTRACT OF THE DISCLOSURE

A computer system that can be operated by a clock frequency higher than the clock frequency by which the critical path instruction is executed correctly. The pipeline is driven at a high clock frequency higher than the clock frequency by which critical path

5   instruction can be executed correctly. The computer system includes a high frequency ALU being operated by the pipeline clock frequency, and at least two low frequency ALUs being operated by the low clock frequency by which the critical path instruction is executed correctly. Each instruction of the execution stage is inputted to the low frequency ALUs alternately and each executes the critical path instruction in two machine

10   cycles. If the high frequency ALU can execute an instruction correctly, the output of the high frequency ALU is selected as the execution result of the pipeline execution stage, and if the high frequency ALU cannot execute an instruction correctly, the output of a low frequency ALU which is in charge of the same instruction is replaced as the execution result of the pipeline execution stage.